APPENDIX E

Characterization of CNRS Fizeau Wedge Laser Tuner

Maryland Univ.
College Park, Md.

Summary:

A new fringe detection and measurement system has been constructed for use with NASA-Goddard's CNRS Fizeau wedge laser tuner, and consists of three circuit boards. The first board is a standard Reticon RC-100B "motherboard" which is used to provide the timing, video processing, and general housekeeping functions required by the Reticon RL-512G photodiode array used in the system. The sampled-and-held video signal from the "motherboard" is processed by a second, custom-fabricated circuit board which a contains a high-speed fringe detection and locating circuit. This board includes a DC level discriminator-type fringe detector, a counter circuit to determine fringe center, a pulsed laser triggering circuit, and a control circuit to operate the shutter for the He-Ne reference laser beam. The fringe center information is supplied to the third board, a commerical single-board computer (SYS-1, manufactured by Octagon Systems Corp.) which governs the data-collection process and interprets the results. The computer begins executing a simple BASIC-language program automatically upon powering up, and this program may be used to communicate the fringe information to an intelligent external controlling device (via an RS-232 interface), or to generate a correction signal directly at the digital output port. The program is stored in a non-volatile on-board EPROM memory which may be erased and reprogrammed as desired.

The following is a summary of the sequence of events involved in making a laser fringe position measurement.

(1) The computer signals the fringe counter board that it is ready to accept data on a new laser shot by dropping the RD (ready for data) line low. This initializes sequencing latches A, B, and C (U8 and U20) and then sets latch A.

(2) At the beginning of the next array scan, the scan START pulse from the array motherboard causes latch B to be set, and the system is ready to acquire fringe data.

(3) As the array readout scan progresses, the signal from the array elements is clocked sequentially onto the VIDEO input, and at the same time a 9-bit binary element counter (U1, U2, and U24) keeps count of the number of the array element being read.

(4) As this process continues, a video discriminator circuit consisting of a X2 amplifier (U11A) and a comparator (U11B) searches for the rising edge of a fringe by comparing the amplified video signal to a preset voltage level.

(5) On the first array element whose video signal exceeds this discrimination level, the comparator switches on the FR (fringe) logic signal, setting latch D (U7) and transferring the count in the element counter to a second 9-bit binary counter (U3, U4, and U25), the fringe center counter. The fringe center counter is incremented once for every two array elements within the fringe, with the result that at the end of the fringe it will contain the location of the fringe center.

(6) As the falling edge of the fringe is read out, the video signal again crosses the preset discriminator level, turning off the FR logic signal and setting latch E. This turns off the fringe center counter and signals the computer that the fringe center counter now contains a valid fringe center location by turning on the VD (valid data) line.

(7) The computer reads and stores this number, opens the helium-neon laser shutter by placing a command on the SH (shutter) line, and begins an analogous process to determine the center of the first helium-neon fringe on the array. The computer then closes the shutter, takes the difference between the test laser and He-Ne reference fringe center locations, prints the result, and the process begins again.

(8) In the event that on a particular array scan there is no fringe detected, either because the laser has not fired or because the video signals lie below the discriminator level, the system simply waits for the next scan containing fringe information.

Design trade-offs:

In terms of both hardware and software design, this system is relatively simple, making it both low in cost and easy to modify. However, this simplicity reflects certain design tradeoffs which should be kept in mind.

First, by virtue of the slow operating speed of the electro-mechanical He-Ne laser shutter mechanism, the measurement throughput rate for this system will be lower than the laser firing rate, perhaps only 1 Hz. For higher speed operation a liquid-crystal light valve or higher-speed electromechanical shutter should be used to switch the He-Ne line on and off. Even with this limitation removed, due to the slow speed of the interpreted BASIC programming language, the system may still fall short of 10 Hz operation unless the program is encoded in assembly language. It should be noted, however, that unless the mechanical feedback device (i.e. motorized micrometer or piezoelectric pusher) servoing the tunable laser can respond with comparable speed, such improvements will have little effect on the response time of the wavelength stabilization process.

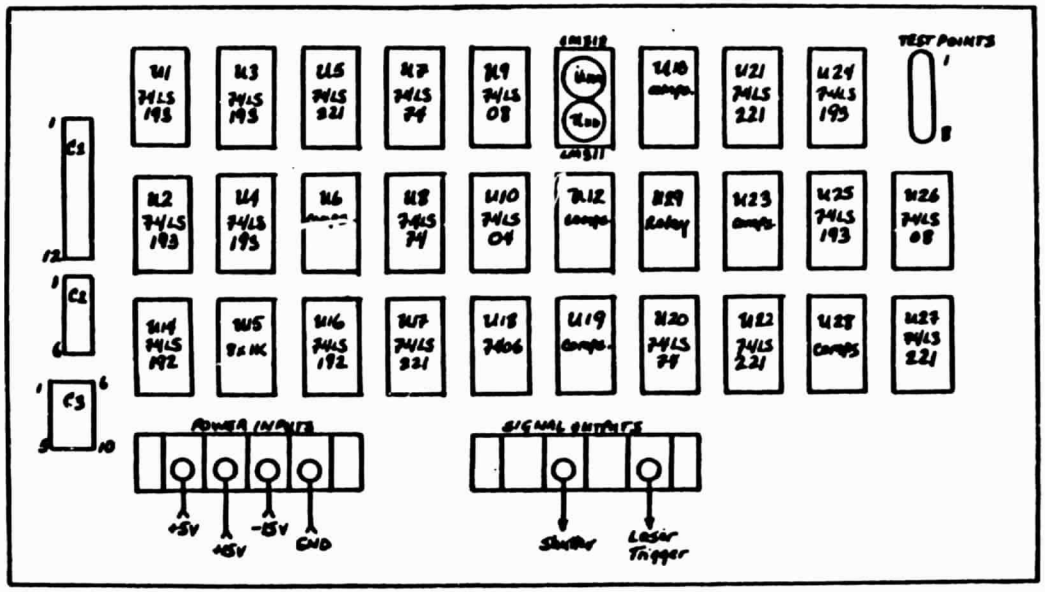
A second consideration arises from the hardware structuring of the fringe detection process. Since a fringe is detected in real time by a DC level-crossing discriminator circuit rather than by storing the scan video information and using digital signal processing techniques, it is a rapid, uncomplicated process. However, since the system considers only the first fringe which is read out on each array scan, the wavelength variation of the laser must not be greater than about half a free spectral range of the wedge in either direction (±0.25 Å) before the fringe walks off the end of the array or another interferometer order emerges at the leading edge. Also, since the discriminator responds only to DC level crossings, the dynamic range of the system is limited by how low one can set the discriminator level before noise is interpreted as fringe data. This noise comes from two sources. First there is optical fringe noise introduced by the characteristic rippled wing structure of fringes from a reflectively coated Fizeau wedge. In the presence of such local peaks the discriminator level must be adjusted high enough to prevent a premature turn-off of the fringe center counters before the actual fringe peak has been crossed. Second, there is electrical noise due to the switching transients and nonlinear response between the individual array elements. There is also a particularly large starting transient on the video line at the beginning of a readout scan, a characteristic of Reticon arrays. To block this transient a video blanking circuit (U27) has been incorporated in the discriminator to clamp the fringe logic (FR) output during the readout of the first 2 or 3 elements of the array. Even with this feature, however, the minimum acceptable fringe signal is typically 25% of the full-scale DC signal level with an optimum adjustment of the level threshold trimpot.

Documentation of Fizeau Wedge Tuner Program

The program listed below is an example of the use of the SYS-1 computer to manage the fringe data collection and readout process. The program is written in National Semiconductor Corp. "Tiny BASIC" which uses a subset of the usual Dartmouth BASIC along with several pseudo-assembly language commands that allow the contents of the I/O registers to be examined and manipulated. The program listing eliminates all superfluous spaces between commands for the sake of execution speed. However, a line-by-line explanation of the program appears below the actual program listing.

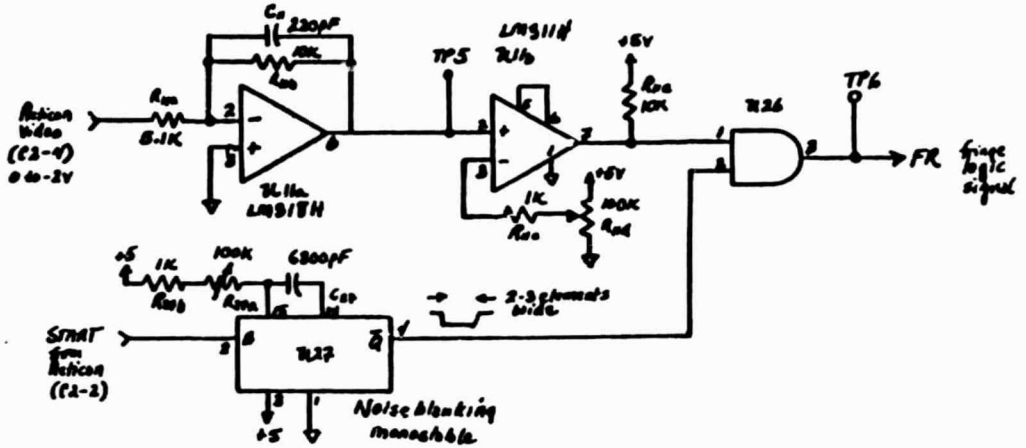
```
10CLEAR
11@#A03+#92
12PR"FIZEAU WEDGE TUNER PROGRAM "
13PR"VERSION 2-24-84 "
14PR"MARK B. MORRIS "
15@#A02=#3
20@#A02=#2
25@#A02=#3
30LETW=@#A01 AND#2
35IFW=0G030
40Y=@#A00
45Z=@#A01 AND#1
50A=Y+Z*256
60@#A02=#1
70@#A02=#0
75@#A02=#1
80LETW=@#A01 AND#2
85IFW=0G080
90Y=@#A00
95Z=@#A01 AND#1
100B=Y+Z*256
115D=A-B
120PRA,B,D
125@#A02=#3
135G020
```

```
10 CLEAR                    ..... ...
                            instruction in an auto-start EPROM.
..
11 @%A03=%92                This configures ports A,B as input ports
                            and port C as an output port.
                            The port addresses are:
                                    Port A (input) = A00
                                    Port B (input) = A01
                                    Port C (output) = A02

12 PR "FIZEAU WEDGE TUNER PGM "
13 PR "VERSION 2-24-84 "        Prints a sign-on message on the TTY.
14 PR "MARK B. MORRIS "

15 @%A02=%3                 This sends a pulse (RD) to the fringe center board
20 @%A02=%2                 to indicate the computer is ready for fringe data.
25 @%A02=%3                 It also initializes the shutter in the closed position.

30 LET W=@%A01 AND %2       Checks for valid fringe data
                            indicated on VD line (bit 1 of port B).

35 IF W=0 GO TO 30          If there is not valid data present, branch
                            back and check again.

40 Y=@%A00                  Load bits 0-7 of fringe center data word
                            from port A to variable Y.

45 Z=@%A01 AND %1           Isolate bit 8 of the data word.

50 A=Y+Z*256                Compose the 9-bit data word.
                            At this point the location of the test
                            laser fringe center has been stored in variable A.

60 @%A02=%1                 This sends a pulse to indicate ready for fringe
70 @%A02=%0                 data and also opens the He-Ne shutter by placing
75 @%A02=%1                 a zero in bit 0 of port B.

80 LET W=@%A01 and %2       Test for valid data.

85 IF W=0 GO TO 80          Loop back and test again if valid data not yet present.

90 Y=@%A00                  Load bits 0-7 of fringe center data word
                            from port A to variable Y.

95 Z=@%A01 AND %1           Isolate bit 8 of data word.

100 B=Y+Z*256               Compose 9-bit data word and store in B.

115 D=A-B                   Take the difference between the test fringe
                            location and the reference fringe location.

120 PR A,B,D                Print laser fringe center, He-Ne fringe center,
                            and the difference between the two locations.

125 @%A02=%3                Close the shutter by placing a one in bit 0 of Port B.

135 GO TO 20                Begin the process again.
```

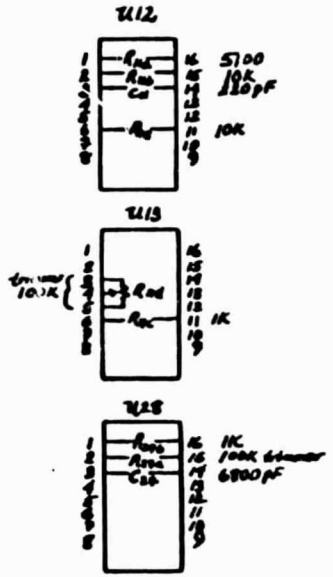


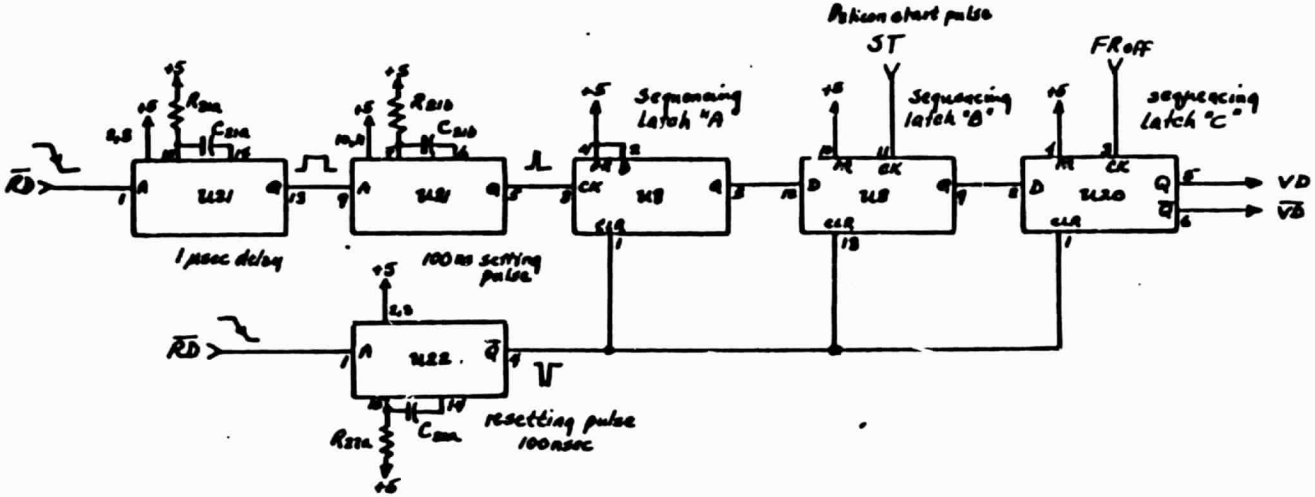
C1 = Ribbon cable to computer card
C2 = Ribbon cable to Rehton motherboard
C3 = Ribbon cable to "LASER REP. RATE" thumbswitches

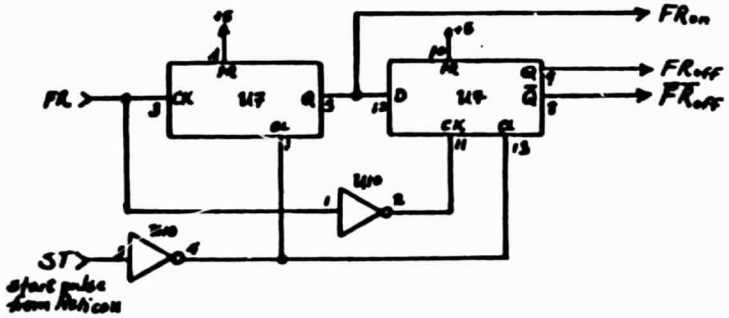
DISCRIMINATOR CIRCUIT WITH NOISE BLANKING



U11a = LM318H op amp
U11b = LM311H comparator
U26 = 74LS08
U27 = 74LS221



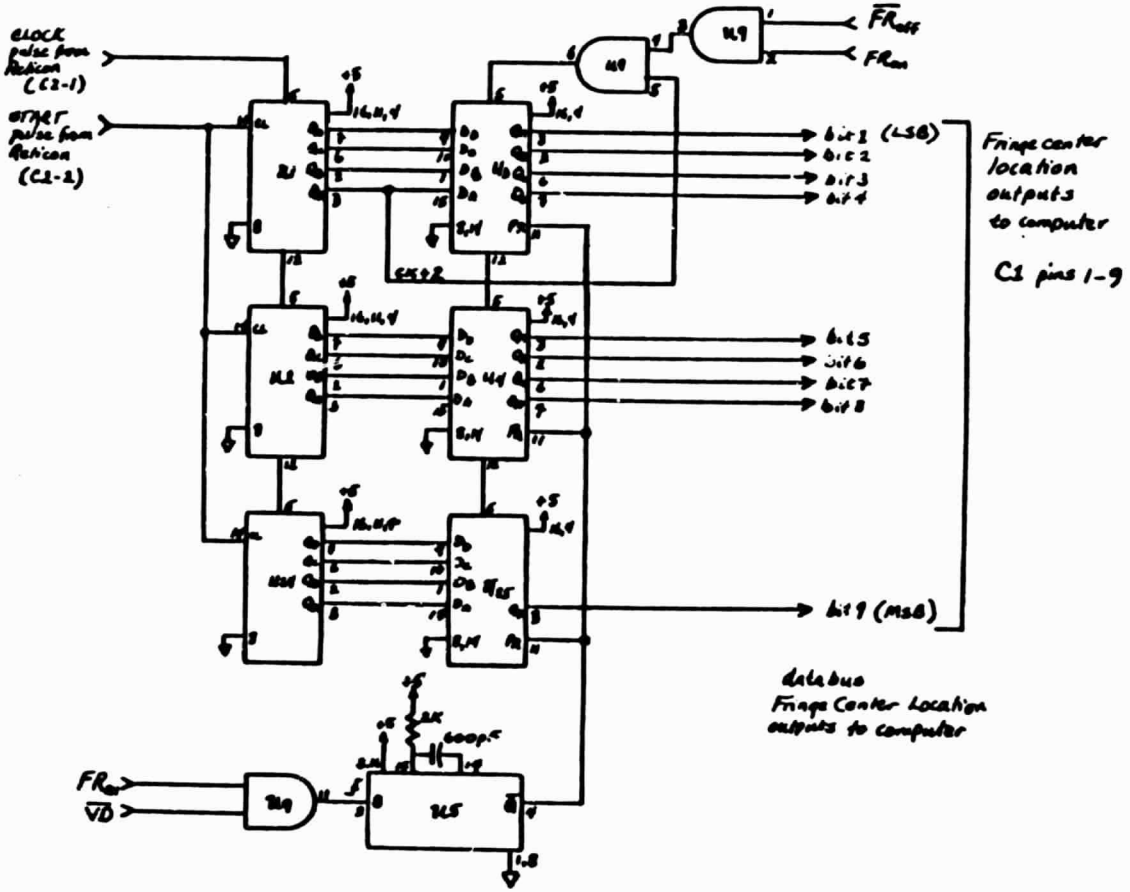




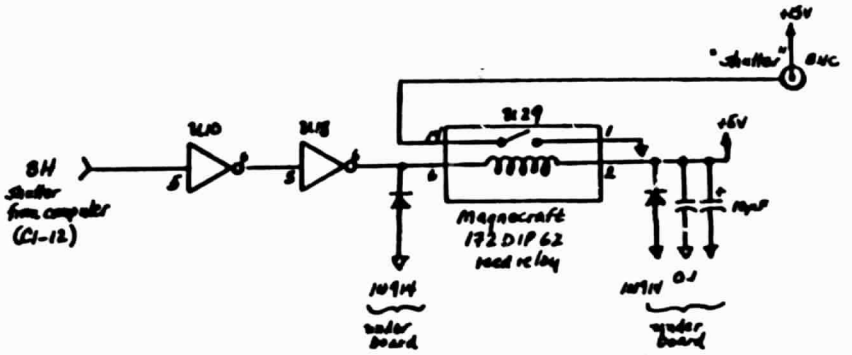
LATCHING / SEQUENCING CIRCUITRY

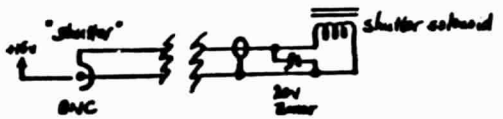
U7 = U9 = U20, 74LS74
U21 = U22, 74LS221

FRINGE CENTER COUNTING CIRCUIT



U1, U2, U24 = 74LS193 are Reticon element counters
U3, U4, U25 = 74LS193 are Fringe center location counters
U9 = 74L308
U5 = 74LS221 Preset pulse generator for Fringe center location counters

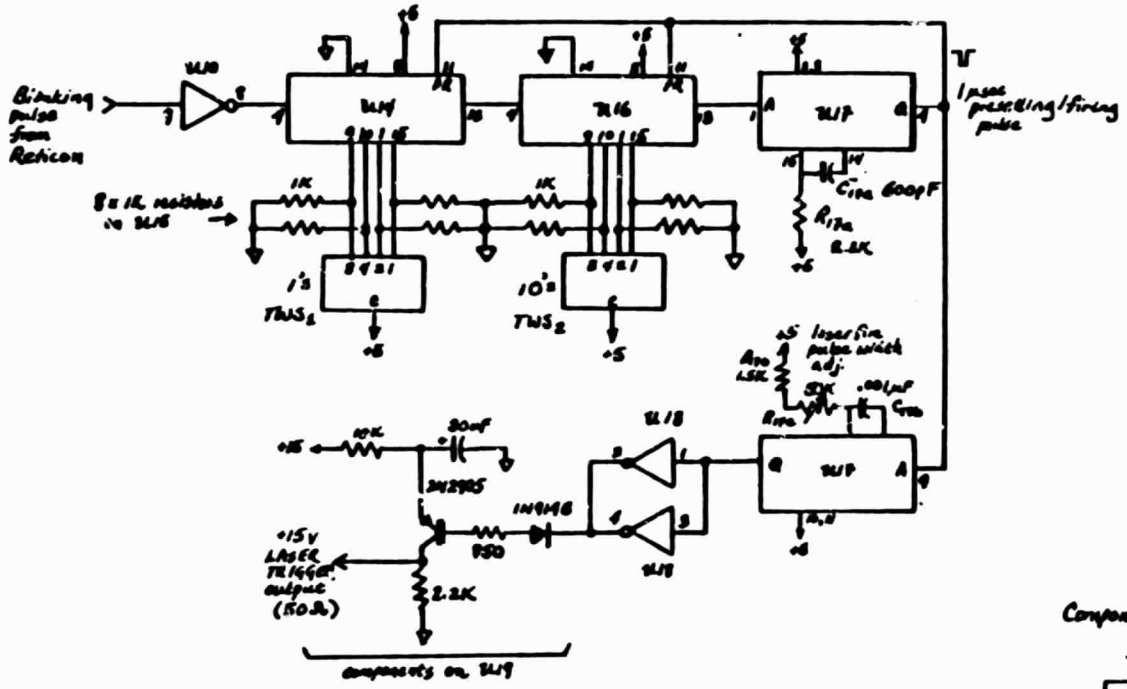




Shutter cable assembly

U18 = 7406
U10 = 74LS04

LASER TRIGGERING CIRCUITRY



U14, U16 = 74LS192 counters

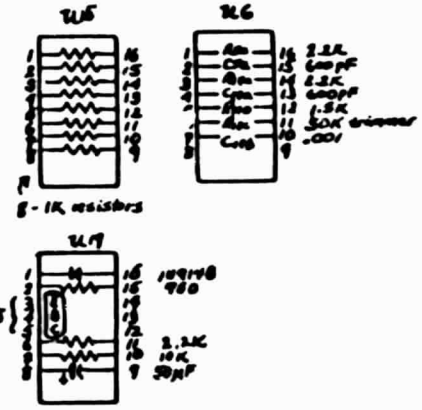
U17 = 74LS221

U18 = 7406

U10 = 74LS04

TWS1, TWS2 = BCD thumbwheel switches

Component carriers



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